Amendments to the Specification:

Please replace the paragraph beginning on page 9, line 24 and ending on page 10, line 4 with the following redlined paragraph:

One embodiment of the decimator 26 is shown in Figure 4 and comprises a shift register 60 and adder 62. The decimator sums N samples together (here 8 samples are summed) to produce an output on line 63. In this example, 8 samples of the digitized received signal are summed giving possible outputs -8 to +8. To represent the possible outputs, the output values 0, 1, 2 or 3 are represented as logic "0" and outputs 5, 6, 7 or 8 are represented as logic "1". To prevent any bias in the output, the value 4 is represented as alternately logic "0" and logic "1". The output on line 63 is therefore a digital bit sequence which is a downsampled version of the digitized received signal without any information being discarded.

Please replace the paragraph beginning on page 10, line 28 and ending on page 11, line 5 with the following redlined paragraph:

Further summing values for N and M are possible. An example of summing an odd number is to shift N = 8 samples at a time into a register of M = 9 bits and sum N = 8. In this example, the eight bit will be summed twice, but we now have no need to have a dither bit as a sum of 0, 1, 2, 3 or 4 is represented as logic ~~A0"~~ "0" and 5, 6, 7, 8 or 9 represented as logic "1" (there are equal chances of logic "0" or "1" occurring). Similarly, division by 17 would involve values 0 to 8 being represented as logic "0" and values 9 to 17 being represented as logic "1".

Please replace the paragraph beginning on page 11, line 18 and ending on page 12, line 2 with the following redlined paragraph:

An incoming signal is mixed down by gate 44, fed with a locally generated 4.092MHz. A decimator 26 comprises combinatorial logic to combine groups of 8 samples to reduce the sample rate without discarding information as before. It is noted, for the avoidance of doubt, that the decimation is not simply removing every 10^{th} sample. The decimated signal is loaded to a shift register 28 having multiple taps 29 which feed to correlators 30. The shift register is operable, when loaded, to circulate at a higher speed than the loading speed, such as

66 MHz or 200 MHz, preferably 128 MHz in one example embodiment. Each tap 29 feeds a separate correlator 30 (only one being shown for simplicity). A code generator 36 generates a local version of the respective CA code and applies this to the correlator 30. The correlator includes combinatorial logic (*e.g.*, multiplexer 32) which combines the local version of the CA code with the decimated received signal from the tap points 29 of the circulating shift register. A low pass filter 34 provides the output.